

- ☒ Projet d'Initiation à la Recherche
- ☐ ☐ Projet d'Innovation-Recherche

Nom du laboratoire ou de l'entreprise/établissement: LAAS/INSA

TUTEUR(S)

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TITRE DU PROJET

Timing analysis for CPU caches with new replacement policies

MOT-CLES

hardware architecture, real-time and embedded systems, cache

DESCRIPTIF (RESUME), indiquer l'enjeu sociétal de l'INSA de Toulouse s'il y a lieu

While the CPU caches are likely to decrease the average program execution times, the worst-case can remain unaffected or even increase. Over the years, the **caches** in **real-time systems** have been disabled due to the lack of appropriate cache-aware worst-case execution time analysis. Such analysis is needed to predict all potential cache misses that can take tens or hundreds of cycles to be resolved and can considerably slow down program execution.

The **cache replacement policy** is a key design parameter that controls the cache runtime behavior. Caching the most recently accessed memory entries is the most common strategy (LRU replacement policy) implemented in the modern general-purpose processors as the programs tend to reuse the data from the same memory region (i.e., spatial locality) over a short period of time (i.e., temporal locality). Such replacement policy, achieving a good hit ratio for most workloads, is, however, susceptible to thrashing (i.e., the useful data is evicted by the incoming data that is not going to be reused) for memory-intensive workloads that have a working set exceeding the cache size. Artificial intelligence and modern computer vision are examples of today's data-intensive applications. Fortunately, many alternative cache replacement policies (e.g., Last-position Insertion Policy (LIP) [1,3]) have been proposed to prevent the cache thrashing in these applications. Whereas the simulation results for the selected applications indicate improved performance, the hard real-time systems require strong deterministic guarantees of timing correctness.

Two different projects can be proposed:

1. The main objective of the first project is to derive the first static **timing analysis** for deterministic caches under one of the alternative cache replacement policies (e.g., LIP). The new analysis can be built on a large body of literature [2] and tools available in the context of the standard replacement policies (e.g., LRU, FIFO, RANDOM). Its implementation can take the form of an extension to the existing frameworks or a new stand-alone tool.
2. The second project aims at **testing different cache replacement policies** on real-world embedded applications (modern computer vision and machine learning). The replacement policies can be implemented in Cachegrind (<https://valgrind.org/docs/manual/cg-manual.html>), which is an open-source cache profiler tool. New cache replacement policies can also be proposed.

[1] M. Qureshi, A. Jaleel, Y. Patt, S. Steely, and J. Emer. 2007. Adaptive insertion policies for high performance caching. SIGARCH Comput. Archit. News 35, 2 (May 2007), 381–391.

<https://people.csail.mit.edu/emer/papers/2007.06.isca.dip.pdf>

[2] M. Lv, N. Guan, J. Reineke, R. Wilhelm, and W. Yi. 2016. A survey on static cache analysis for real-time systems. Leibniz Transactions on Embedded Systems, vol. 3, no. 1. p. 05:1-48.

<http://user.it.uu.se/~yi/pdf-files/2016/lgyrw-acm15.pdf>

[3] B. A. Araujo, G. Gracioli, T. Kloda, D. Hoornaert and M. Caccamo, "Implementation and Evaluation of Adaptive Cache Insertion Policies for Real-Time Systems," 2021 XI Brazilian Symposium on Computing Systems Engineering (SBESC), Florianopolis, Brazil, 2021, pp. 1-8, doi: 10.1109/SBESC53686.2021.9628309.

PROFIL DES ETUDIANTS SOUHAITE (1 seul choix par projet)

- ☐ AE-SE : spécialité Automatique-Electronique parcours Systèmes Embarqués
- ☒ IR-SI : spécialité Informatique parcours Systèmes Informatiques
- ☒ IR-SC : spécialité Informatique parcours Systèmes Communicants
- ☒ (optionnel) ce projet peut être proposé à un ou des étudiants d'échange sur la partie réalisation seule (semestre 1 et/ou semestre 2)

PRIORITE : 2

